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13. ABSTRACT *(Maximum 200 words)*

During the course of this two-year program, the first silicon-on-gallium arsenide, SonG, wafers were successfully produced. These Si-on-GaAs (SonG) wafers were shown to be able to withstand temperature cycles to in excess of 700°C, and thus to be suitable for CMOS fabrication using a reduced-temperature SOI process and for epitaxy-on-electronics (EoE) integration of optoelectronic devices using molecular beam epitaxy. GaAs-based quantum-well heterostructures with high photoluminescent efficiency and narrow emission line shape were grown by molecular beam epitaxy in windows cut through to the gallium arsenide substrate on SonG wafers, demonstrating the feasibility of doing EoE processing on this foundation. Substantial progress was made before the end of the program in developing techniques to planarize processed CMOS wafers sufficiently for wafer bonding, but the results were not sufficiently developed that reliable bonding of CMOS on GaAs could be demonstrated. This work is continuing with other funding.

14. SUBJECT TERMS

Optoelectronic integration; gallium arsenide; wafer bonding; epitaxy-on-electronics

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Final Progress Report

Monolithic Integration of Optoelectronic Devices and Si-CMOS on Gallium Arsenide

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Date: November 15, 2000

Statement of Problem Studied:

Researchers have long recognized the desirability of monolithically integrating III-V semiconductor optoelectronic devices, such as laser diodes and p-i-n detectors, with complex high density, high performance silicon electronic integrated circuits, ideally CMOS, to economically produce robust optoelectronic integrated circuits for a wide variety of applications. To this end, work was begun many years ago growing GaAs epitaxially on silicon, and this GaAs-on-Si research continues to this day, but with limited success. While most people focus on the lattice constant mismatch between Si and GaAs (and other III-V's) as the main difficulty with this approach, the more important issue is the large difference in thermal expansion coefficient (TEC) between these materials. Very large stresses are induced in epitaxial III-V layers on silicon by even relatively small temperature changes because of the TEC difference; and such stresses are fatal to many optoelectronic devices.

We feel that the key to III-V/silicon monolithic optoelectronic integration lies in recognizing that optoelectronic devices are intrinsically very thick devices (typically at least a micron thick) which are very sensitive to stress, and silicon MOS transistors need only be a few tens of nanometers thick and are much less stress sensitive. Silicon-on-insulator, SOI, transistors, for example, are routinely formed in Si films less than 10 nm thick. It is also well known from silicon-on-sapphire, SOS, processing that such thin silicon can withstand very high stresses induced by a large difference in TEC, in this case between Si and sapphire (which has a TEC similar to that of GaAs.)

Clearly the solution to monolithically integrating Si CMOS and GaAs-based optoelectronics is (1) to take advantage of the fact that one is not restricted to using silicon as the substrate for Si CMOS, and (2) to retain a GaAs substrate so that the intrinsically thick, inherently strain- and defect-sensitive optoelectronic devices see their optimum substrate, i.e., GaAs. In particular one can imagine using wafer bonding and SOI techniques to produce Si CMOS electronics on gallium arsenide substrates without sacrificing any of the performance of the CMOS while at the same time

gaining access to state-of-the-art performance optoelectronic devices, e.g. laser diodes and photodetectors. This is the approach we are pursuing in developing a technology we term Silicon-on-Gallium Arsenide (SonG). The SonG process combines silicon and gallium arsenide substrates by wafer bonding. It builds expertise at MIT in the areas of wafer bonding, silicon on insulator (SOI) MOS IC technology, and epitaxy on electronics (EoE) optoelectronic integration technology [1].

The objective of this specific research was to demonstrate that silicon integrated circuits can be monolithically integrated with GaAs-based optoelectronic devices by using wafer bonding techniques to create silicon-on-gallium arsenide (SonG) wafers suitable for processing SOI CMOS and for use as substrates for optoelectronic device epitaxy. The innovation is to make the Si no thicker than needed for CMOS (i.e., 100 nm or less) so that it will be highly resistant to thermal expansion stresses, and to place it on the GaAs substrates needed to make reliable, long-life laser diodes.

<u>Summary of Most Important Results</u>:

During the course of this two-year program, the first silicon-on-gallium arsenide, SonG, wafers were successfully produced [2]. SIMOX silicon-on-insulator, SOI, wafers were bonded to oxide-coated GaAs wafers and the substrate of the SOI wafer was etched away, leaving a thin, single crystal Si layer intimately bonded to the full-thickness GaAs wafer. Specifically, 100 nm thick silicon single crystal layers were bonded by intervening oxide layers on 4" diameter GaAs wafers.

These Si-on-GaAs (SonG) wafers were shown to be able to withstand temperature cycles to in excess of 700°C [2], and thus to be suitable for CMOS fabrication using a reduced-temperature SOI process and for epitaxy-on-electronics (EoE) integration of optoelectronic devices using molecular beam epitaxy.

GaAs-based quantum-well heterostructures with high photoluminescent efficiency and narrow emission line shape were grown by molecular beam epitaxy in windows cut through to the gallium arsenide substrate on SonG wafers, demonstrating the feasibility of doing EoE processing on this foundation [3].

The same process used to create Si-on-GaAs wafers can also be used to transfer fully-processed SOI CMOS circuits to GaAs wafers (to be followed by EoE optoelectronic integration). To this end, eight-inch diameter fully processed SOI CMOS wafers were obtained from IBM [4] and four-inch diameter wafers compatible with processing and wafer bonding equipment available to the program at MIT were laser-cut from these wafers [5]. Substantial progress was made before the end of the program in developing

techniques to planarize processed CMOS wafers sufficiently for wafer bonding, but the results were not sufficiently developed that reliable bonding of CMOS on GaAs could be demonstrated.

Work is continuing under a different program to planarize and bond processed SOI CMOS wafers to GaAs wafers using the SonG process. This is the master's degree thesis research of Mr. Ed Barkley. Success in this area will open the way subsequently for the full integration of III-V light emitters (LEDs and laser diodes) with silicon CMOS electronics.

<u>List of Publications and Technical Reports</u>:

Joanna M. London, Andrew H. Loomis, Joseph F. Ahadian, and Clifton G. Fonstad, Jr., "Preparation of silicon-on-gallium arsenide wafers for monolithic optoelectronic integration," IEEE Photonics Technology Letters, Vol. 11 (1999) 958-960.

Joanna M. London, Pablo Aitor Postigo, and Clifton G. Fonstad, Jr., "Quantum well heterostructures grown by molecular beam epitaxy on silicon-on-gallium arsenide substrates," App. Phys. Lett., Vol. 75 (1999) 3452-3454.

Joanna M. London, "Wafer Bonding for Monolithic Integration of Si CMOS VLSI Electronics with III-V Optoelectronic Devices," S.M. Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, June 1999 (unpublished, copy available on request).

Joseph F. Ahadian, "Development of a Monolithic Very Large Scale Optoelectronic Integrated Circuit Technology," Ph.D. Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, January 2000 (unpublished, copy available on request).

Wojciech Piotr Giziewicz, "Optoelectronic Integration Using Aligned Metal-to-Semiconductor Bonding," S.M. Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, June 2000 (unpublished, copy available on request).

<u>List of Participating Scientific Personnel</u>:

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Joseph F. Ahadian, Graduate Research Assistant, Ph.D. candidate, degree received in January 2000

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Wojciech Piotr Giziewicz, Graduate Research Assistant, S.M. candidate, degree received in June 2000

Joanna M. London, Graduate Research Assistant, S.M. candidate, degree received in June 1999

Report of Inventions:

"Silicon on III-V Semiconductor Bonding for Monolithic Optoelectronic Integration," specification filed on July 14, 2000 as Application Serial No. 09/616,456 (Docket No.: MIT7942), Inventors: Clifton G. Fonstad, Jr., Joanna M. London, and Joseph F. Ahadian.

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1. Clifton G. Fonstad, "Very Large Scale Monolithic Heterogeneous Optoelectronic Integration: the Epitaxy-on-Electronics, Silicon-on-Gallium Arsenide, and Aligned Pillar Bonding Techniques" in Heterogeneous Integration: Proceedings of a Conference held January 25-26, 2000 in San Jose, CA edited by Elias Towe (Critical Reviews of Optical Engineering, Vol. CR76, SPIE Optical Engineering Press, Bellingham, WA, 2000) Chapter 1.

2. Joanna M. London, Andrew H. Loomis, Joseph F. Ahadian, and Clifton G. Fonstad, Jr., "Preparation of silicon-on-gallium arsenide wafers for monolithic optoelectronic integration," IEEE Photonics Technology Letters, Vol. 11 (1999) 958-960.

3, Joanna M. London, Pablo Aitor Postigo, and Clifton G. Fonstad, Jr., "Quantum well heterostructures grown by molecular beam epitaxy on silicon-on-gallium arsenide substrates," App. Phys. Lett., Vol. 75 (1999) 3452-3454.

4. Wafers supplied by Dr. Fariborz Assaderaghi, IBM, East Fishkill, NY.

5. Laser cutting performed by Laser Services, Inc., 123 Oak Hill Road, Westford, MA 01886.